/ Descriptions

EUF P 57F49VF ĩ VRS0 ; Ł [OBJ] ¸ 49 Nel₩ Ł±F [OBJ] ч Φ ɔ ؕ ح è ṇ
The BRCM24C16SC is 16Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. HF Product Code.

/ Features

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ѡ ɔ Ⱨ₆ 41 : Y ɔ 518~818Y ڑ ѡ `Hت ¦ ' 4 P k} ɔ 41 : ~518Y ڑ
ѡ `Hت ¦ ' 733Nk} ψ
Ⱨ ı ă F P RV ح ɔ ╚ 733xD ε ѡ ζ ɔ ╚ 419 p D ε ѡ ζ ψ
Ạ ≠ Ն ▾ └ ڑ Ҍ ψ
˚ ₰ ح ≠ ψ
49 È ` ˜ ₩ ψ
è ʗ˚ [OBJ] ψ
ڳ ɾ ح ˜ 45 ; ч ˚ ᴺ ψ
₅ `H Ϙ ε ѡ 8 p v ζ ψ
ᴝ ˛ χ ح ₭ 433 ₭ è 433 ẉ HVG ε KE P ₩ ζ Ĩ χ 9NY ح Ĩ
χ . 20533 p D›
Single Supply Voltage
Minimum operating voltage down to 1.7V 1 MHz clock from 2.5V to 5.5V 400kHz clock from 1.7V to 2.5V
Low power CMOS technology Read current 400uA, maximum Write current 1.6mA, maximum
Schmitt Trigger, Filtered Inputs for Noise Suppression
Sequential & Random Read Features
16-byte Page Write Modes
Write protect of the whole memory array
Additional Write Lockable Page and 128-bit Serial Number
Self-timed Write Cycle (5ms maximum)
High Reliability Endurance: > 1 Million Write Cycles Data Retention: > 100 Years HBM: 6KV
Latch up Capability: +/-200mA;

/ Applications

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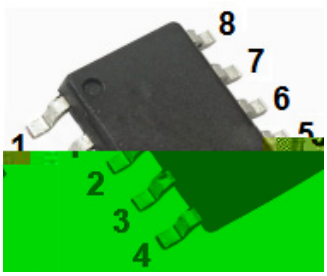
Household appliances, Network communications, Portable Bluetooth devices, Set-top boxes, Smart meters, Fingerprint unlocking devices

/ Pinning





/ Pinning

Slq	Qdph	W|sh	Ghvfulswlrq
4	QF	0	Ɯ
5	QF	0	Ɯ
6	QF	0	Ɯ
7	JQG	Jurxqg	ϟ Ɑ
8	VGD	L2R	Φ ڑ 2ڑ
9	VFO	Lqsxw	Φ`Hٹ ڑ
:	ZFE	Lqsxw	Ḥ ɔ Ẉ ΐ
;	YFF	Srzhu	ɔ ◊ ΰ

/ Marking

ð ɿ ب ˝ / See Marking Instructions

/ Absolute Maximum Ratings(Ta=25)

Parameter	ɿ N Symbol	Rating	ϑ Unit
Storage Temperature	T_{stg}	-65~+150	
Operation Temperature	T_{opr}	-40~+85	
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ ε Vcc+1.0 ζ	V
DC Output Current	I_{out}	5.0	mA
Electro-Static discharge HBM mode	ESD	6000	V

/ Reliability Characteristic

Parameter	ɿ N Symbol	⊥⊥ ؛ ɨ Test Conditions	ω Min	ε Typ	ω Max	ϑ Unit
Endurance	EDR	25 3.3V Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

Parameter	ㄚ N Symbol	ㄦ ;ㄔ Test Conditions	ω Min	ε Typ	ω Max	ϑ Unit
Supply Voltage	Vcc		1.7		5.5	V
Standby Current	Isb	Vcc = 3.3V, TA = 85¯C			1.0	uA
		Vcc = 5.5V, TA = 85¯C			3.0	uA
Supply Current	Icc1	Vcc=5.5V, Read at 400Khz		0.2	0.4	mA
Supply Current	Icc2	Vcc=5.5V,Write at 400Khz		0.8	1.6	mA
Input Leakage Current	ILI	VIN = Vcc or GND		0.1	1.0	uA
Output Leakage Current	ILO	VOUT = Vcc or GND		0.05	1.0	uA
Input Low Level	VIL		–0.6		0.3Vcc	V
Input High Level	VIH		0.7Vcc		Vcc+0.5	V
Output Low Level Vcc = 1.7V (SDA)	VOL1	IOL = 1.5 mA			0.2	V
Output Low Level Vcc= 3.0V (SDA)	VOL2	IOL = 2.1 mA			0.4	V

1.7V≤

ㄚ N

Parameter Symbol

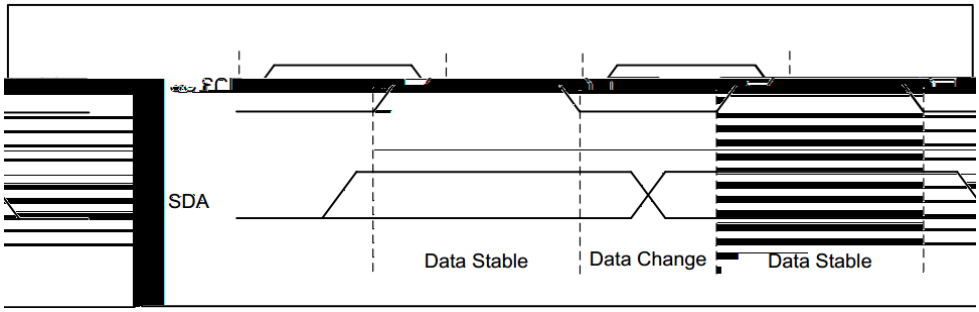
Parameter	Symbol	1.7V≤Vcc<2.5V			2.5V≤Vcc≤5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	us
Data In Setup Time	t							

/ Functional Description

/ Data Input

VGD ǖ ڼ ɤ ɯɦ ɸ ɤ VGD ǖ i ǖ ǐ VF0 Ḥ ɔ Ẉ`H ˜ + 4 ˜ , VF0 ɤ ɔ Ẉ Ǫ ɟ VGD ɨ ɣ N ƀ N + 4 ˜ , χ

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

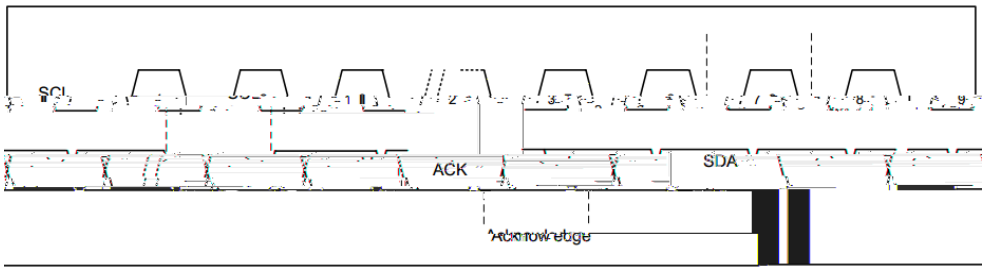


Il j xuh 4 Gdwd Ydolglw|

/ Start Condition

/ Functional Description

All addresses and data words are serially transmitted to and from the BRCM24C16SC in 8-bit words. The BRCM24C16SC sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.



/ Functional Description

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C16SC	Normal Area	1	0	1	0	P2	P1	P0	R/W
	ID Page	1	0	1	1	X	X	X	R/W
	Lock Bit	1	0	1	1	X	X	X	R/W
	Serial Number	1	0	1	1	X	X	X	1

/ Functional Description

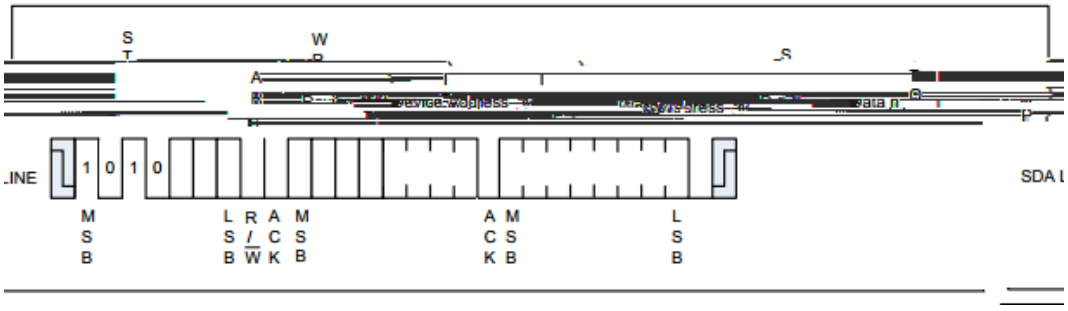


Figure 5 Byte Write

/ Page Write

ˇ ˛ ЛЬ È ` ˀ ĩ Ɑ ⅄ Ꝁ j ˇ ₿ ˀ ɲ
EUF P 57F49VF ⅄ È ` Ɑ Ɋ ⅄ ⅄ ˇ ˜ ⊡ È EUF P 57F49VF ⅛
È ` ʖu ⊣ ɒ 3 ɓ ⅄ Ɑ Ɋ ⅄ ⊣ ₿ ⅄ ⅄ ˇ

A page write is initiated the same as a byte write<a3ut the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C16SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C16SC will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.



Figure 6 Page Write

⅛ È È ⊡ Ḥ 7 ɥ ʊh ɲ ɔ ɛ È ɥ j ɲ ɒ è ˇ
Φ ɥ ⅃ ʊh ⊣ ⊡ È ˇ ˇ ˇ ˇ ⅄ ˇ ⊡ È ` ˇ ⊡ ˇ ˇ
EUF P 57F49VF ⊡ È ⅄ ص 49 ˇ È ˇ چ ⊡ ɋ ʅu ˇ ˇ Ω ˇ ⊡

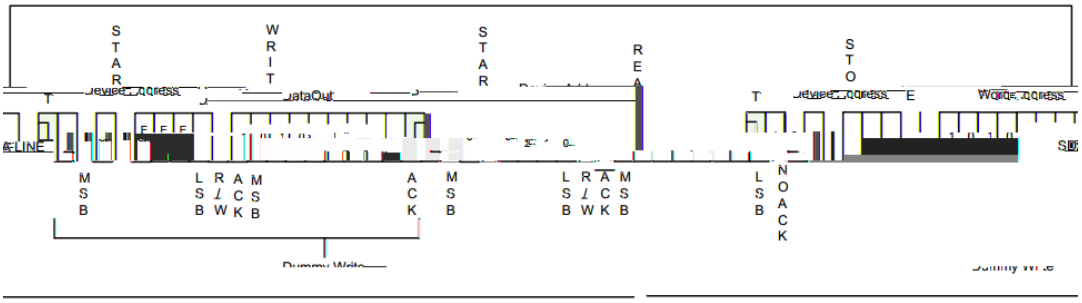
/ Functional Description

/ Acknowledge Polling

ñ ɯ̃ ̀H Ω ̃ ̀ ɾ EUF P 57F49VF ɽ ɷ ɴ ɔ̃ ɸ ɣ ɴ ˁ ɸ È ̀ ˍ ح 2 ɥ Ɱ ˊ ɹ ⓞⓑⓙ ω̃ ɯ̃ Ω EUF P 57F49VF ɒ 3 ɓ ɒ ح ˚ ʌ ʌ

Once the internally timed write cycle has started and the BRCM24C16SC inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the BRCM24C16SC respond with a “0”, allowing the read or write sequence

/ Functional Description

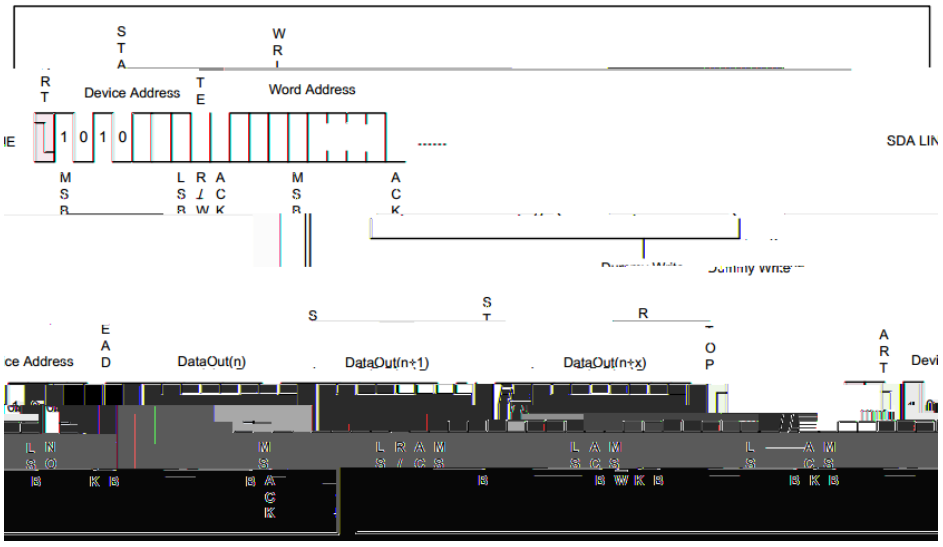


Ilj xuh ; Udqg r p Dgguhvv Uhdg

/ Sequential Read

ْ ح ٰ ح ﻫ ح È ﷺ ﻟ ﻟ ﻟ
EUF P 57F49VF ﻟ ﻟ ﻟ ﻟ È Φ ﻟ ْ È ` ﻟ è ﻟ
`H È ˇ ﺟ ْ ح ﻟ ﻟ ≡ ω̃ ɒ 3 ɓ ﻟ ฿ N `H ْ
ح ﻟ ฿ ε < ˜ ζ

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C16SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).



Ilj xuh < Sequential Read

/ Functional Description

/ Read Identification Page

‰ ˇ ˘ ε 49 È ` ζ ĩ ˇ ˘ ˘ ˛ Ω ح ₩ ï ⇔ ج ˇ ˘ ˘ ˛ Ω ن ص ح ˇ ˘ ˘ ˛ ⊓ ح أ ⊓ ⊓ ⊓ ح ⊓ ε ⊓ ⁵ è ˚ ζ ω̃ ⊡ ⊓ ⊤ ⊕ ⁴ ‰ ˇ ˇ ⊖ 4344e ⊔ D : 2 D9 ء 3 ᾰ D8 ⊔ D7 2 D3 ⊖ ‰ ˇ ˘ ⊡ È ` ⊔G ˘ ˛ ⊔ ح ⊡ È ` j ⊼ ص ˘ ˛ ژ ⊓ ε ⊔ ⊥ 43g ح ‰ ˇ ˘ ˘ H È ` ⊣ 9 ⊔G ˘ ژ ⊓ 49 È ` ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page c

/ Functional Description

% ° N È D: D9 ɥ ° ɒ 43 ɓ ´ 5 ˜ Ĺ ɸ ' ɤ ɒ 43 ɓ Ɋ È ɑ ψ ɸ ʒ ' Θ ε ˜ χ ' ɤ ˥ `Ω ح ° N ˥ È ` ¸ È ʒ ɹ ɭ ;3k ζ ʒ 45; ɥ ε 49 È ` ζ ° N `H ʌ ʌ ح è Ṁ7 ɥ ° N ح È ˘ ج 45; ɥ ° N È ≡ ω ɹ ε DFN ζ `H ° N ح ʌ ฿ ฿ ε ɤ : ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

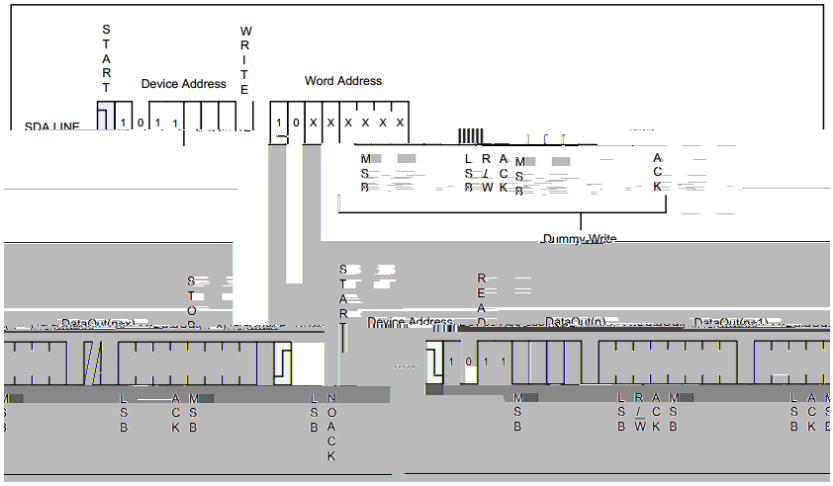
Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 on page 9, de8ummy write, andthe use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, de8ummy write sequence, ds part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation wds to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a „10□ sequence in bit A7 and A6 of the word address, regardless of the intended address ds depicted in Table 2 on page 9. If a word address other than „10□ is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

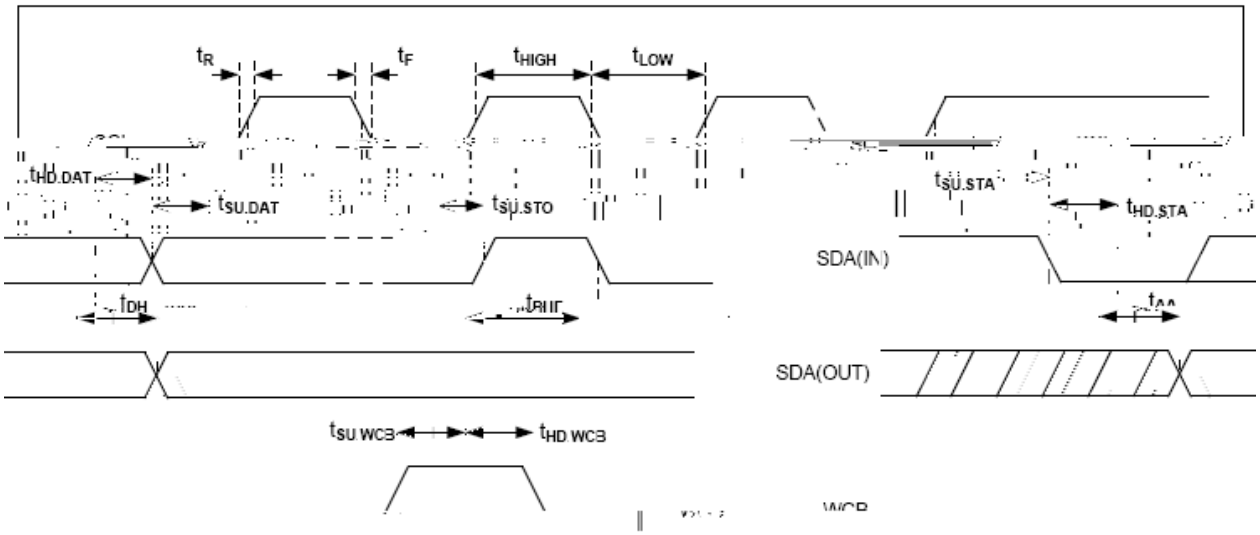
When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)



Il j xuh 44 Vh t xhqwld0 Uhdg

/ Time Sequence Diagram

Bus Timing

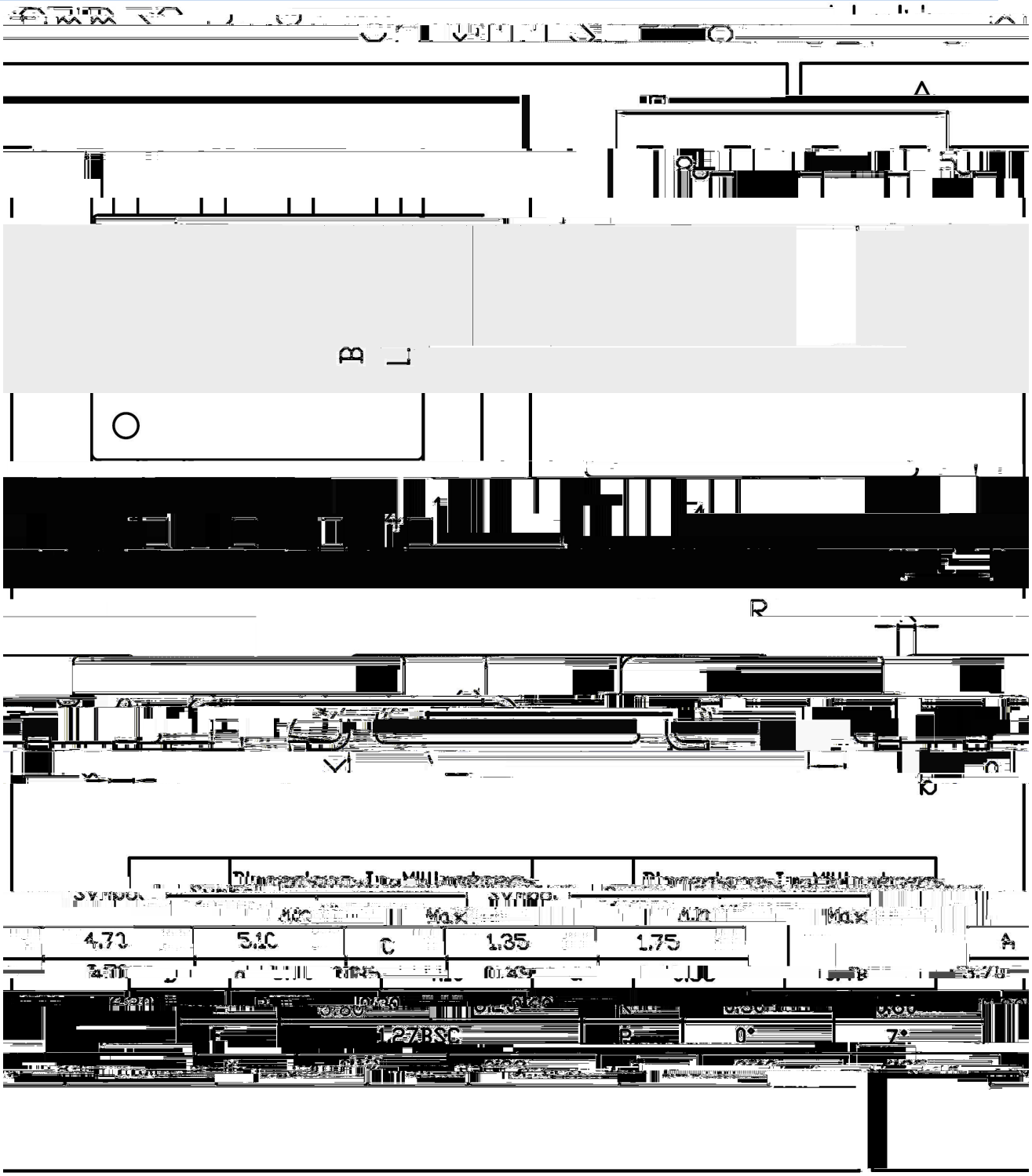


Write Cycle Timing

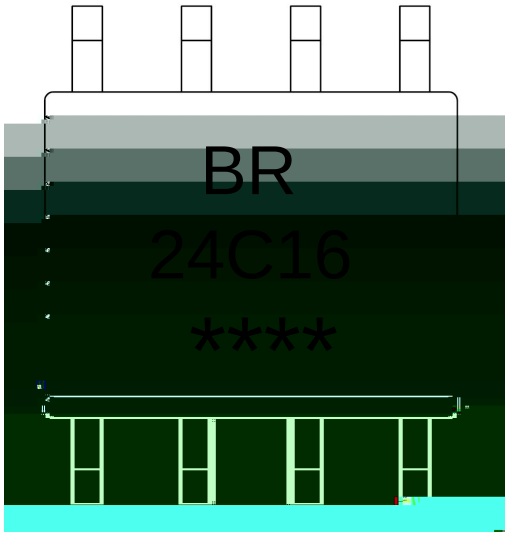


Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

/ Package Dimensions



/ Marking Instructions



ب ˝ χ

BR χ ᴎ Ɱ

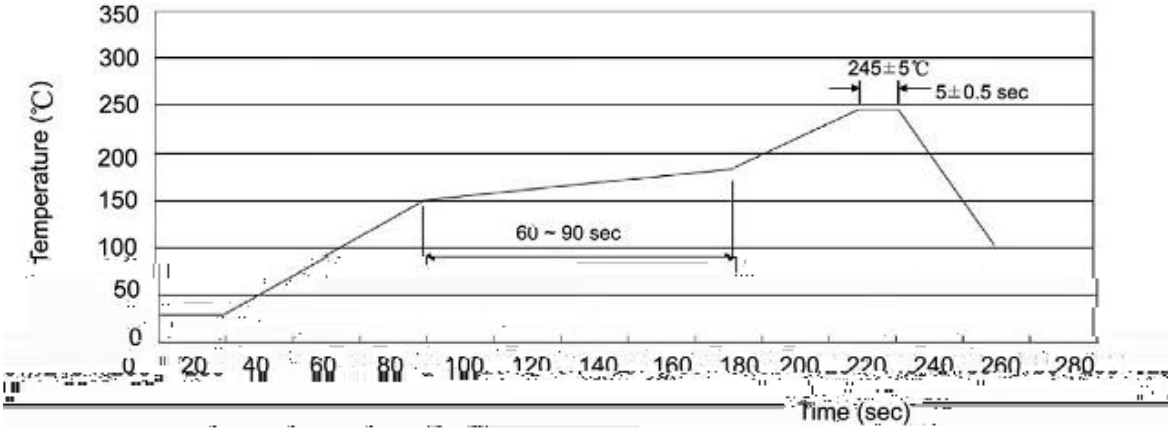
57F49 χ ᴺ Ɱ

---- χ ᴵ ᴺ Ɱ ɵ ᴵ ᴺ

Note:

BR:	Company Code.
24C16:	Product Type.
****:	Lot No. Code, code change with Lot No.

( ) / Temperature Profile for IR Reflow Soldering(Pb-Free)



ب ˝ χ

1 أ ♬ □ 150 180 `H ژ 60 90sec;

2 □ 245 ° 5 `H ژ ﻫ 5 ° 0.5sec;

Note:

1.Preheating:150~180 , Time:60~90sec.

2.Peak Temp.:245 ° 5 r5 o• T Ð \ `ÐÀ;Ð