BRCM24C32SC SOP-8 32 Kbit I²C

The BRCM24C32SC is 32Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. Halogen-free Product.

1.7V 2.5~5.5V 1Mhz 1.7~2.5V

400Khz

CMOS 400uA 1.6mA

ر V q.2 ộ 15AN

Pin	Name	Type	Description
1	E0	Input	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

/ See Marking Instructions

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{stg}	-65~+150	
Operation Temperature	T_{opr}	-40~+85	
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ Vcc+1.0	V
DC Output Current	I_{out}	5.0	mA
Electro-Static discharge HBM mode	ESD	6000	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Endurance	EDR	25 3.3V Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

		1.7V≤Vcc<2.5V	2.5V≤Vcc≤5.5V	
Parameter	Symbol			Unit

p

SDA SDA SCL (1) SCL
SDA (1)

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

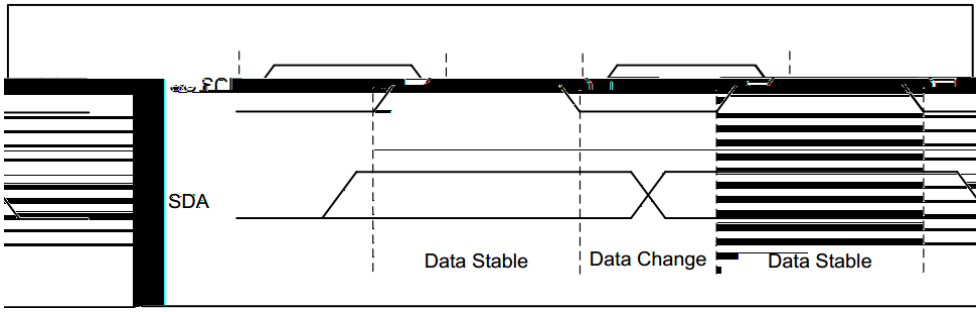

Figure 1 Data Validity

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SCL SDA
2

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

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SCL SDA
BRCM24C32SC

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C32SC in a standby power mode (see Figure 2).

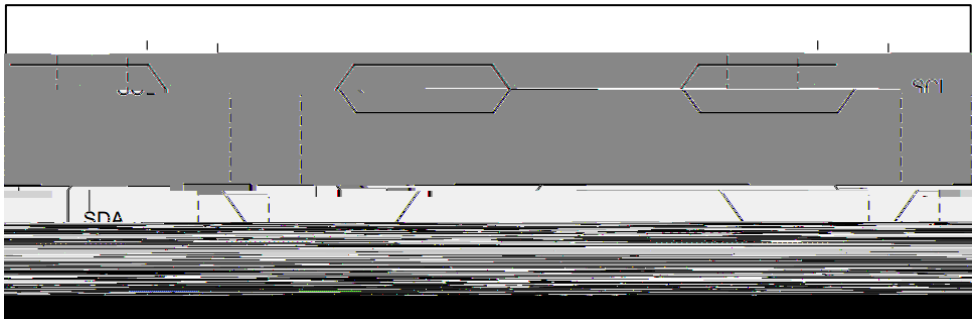

Figure 2 Start and Stop Definition

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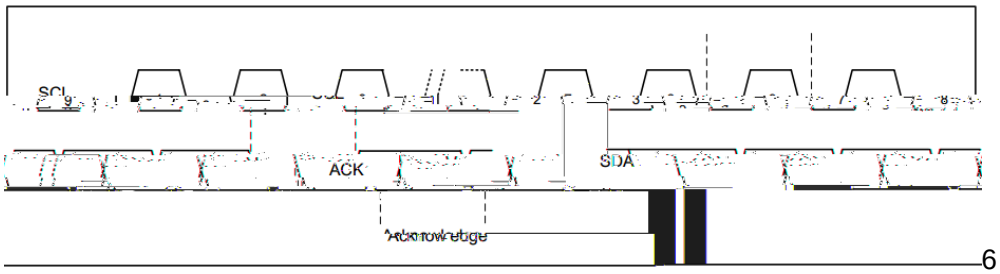
BRCM24C32SC BRCM24C32SC “ 0 ”
ACK 9

All addresses and data words are serially transmitted to and from the BRCM24C32SC in 8-bit words. The BRCM24C32SC sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.



Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	X	X	X	X	A11	A10	A9	A8
	ID Page	X	X	X	X	0	0	X	X
	Lock Bit	X	X	X	X	X	1	X	X
	Serial Number	X	X	X	X	1	0	X	X

Table 2 First Word Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C32SC	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	X	X	X	A4	A3	A2	A1	A0
	Lock Bit	X	X	X	X	X	X	X	X
	Serial Number	X	X	X	X	A3	A2	A1	A0

Table 3 Second Word Address

E2 E1 E0 8 E2 E1
E0 8 /
0 1 0

The E2, E1 and E0 device address bits to allow as many as 8 devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2, E1 and E0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

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BRCM24C32SC WCB Vcc
BRCM24C32SC has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

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8
BRCM24C32SC “ 0 ” 8 8
BRCM24C32SC “ 0 ”
BRCM24C32SC BRCM24C32SC
(5)

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the BRCM24C32SC, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

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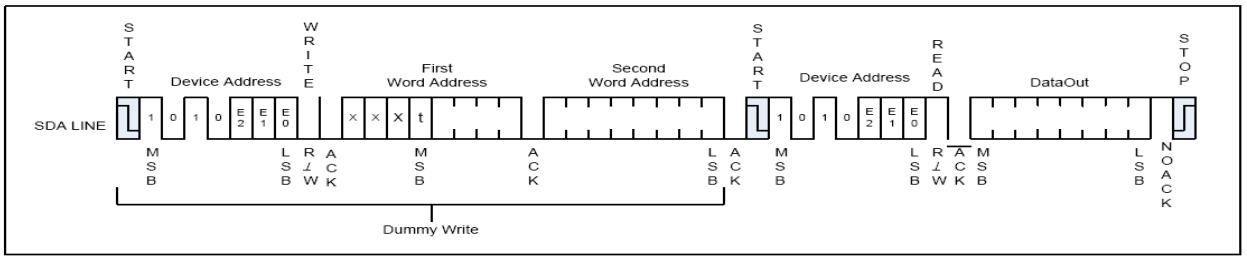
BRCM24C32SC

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BRCM24C32SC,the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BRCM24C32SC acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).



Notes: [1] x means don’t care bits.

[2] t means don’t care bit for BRCM24C32SC

Figure 8 Random Address Read

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BRCM24C32SC

“ 0 ”

9

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C32SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

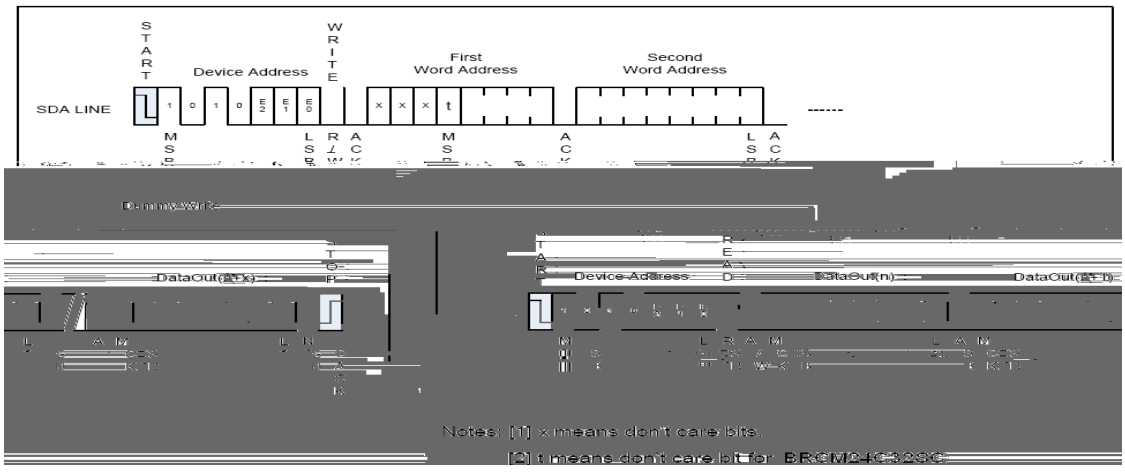

Figure 9 Sequential Read

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32

1011b A15 / A5 A4 / A0 ID

10d 22 ID

32

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

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[+] /

ACK NoACK,(10)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked (see Figure 10).

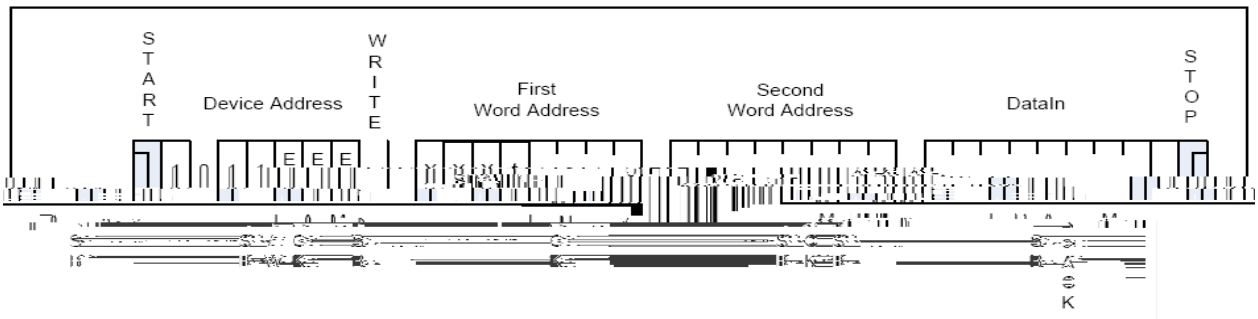

Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

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1

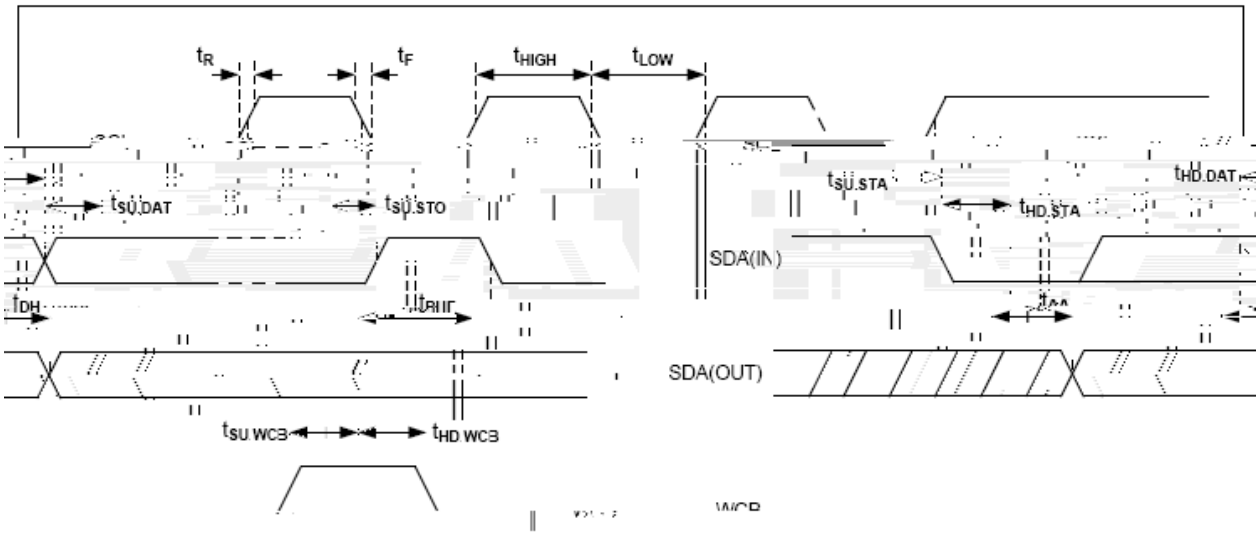
128

EEPROM " "

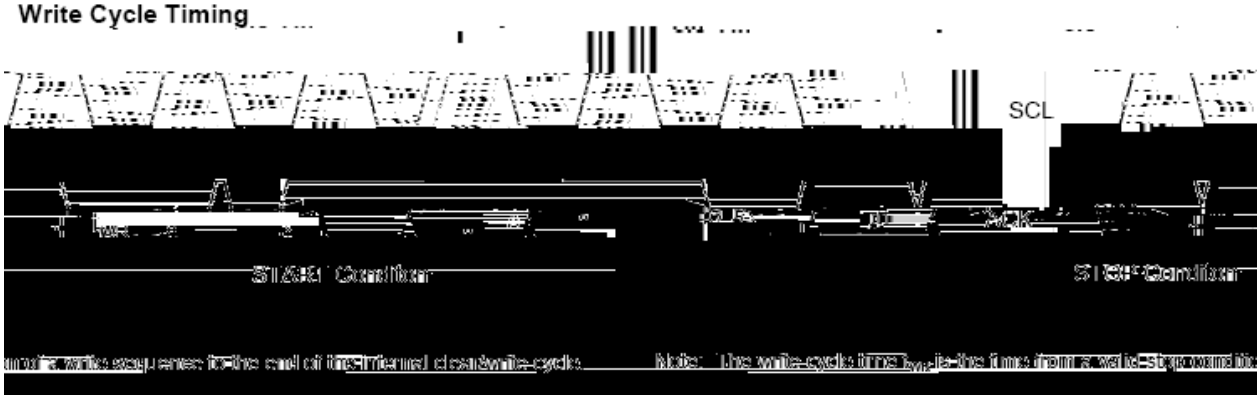
EEPROM

1

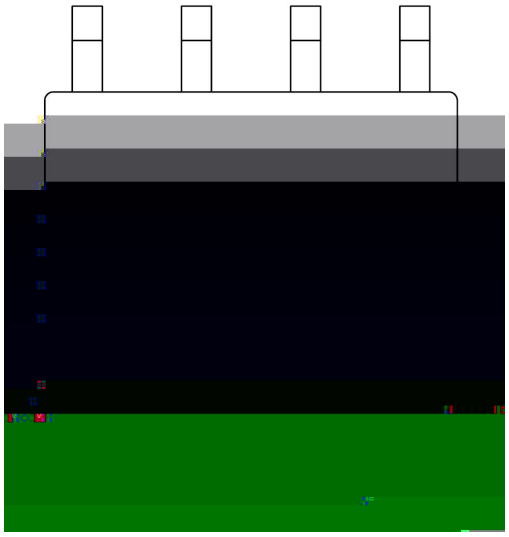
Bus Timing



Write Cycle Timing




A
B
L
E
R
A
4.70
5.10
C
1.35
1.75
1.27BSC
0°
7°



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24C32

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Note:

BR: Company Code.

24C32: Product Type.